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(54) Method of fabricating semiconductor device capable of providing mosfet which is improved in a threshold voltage thereof

(57) In a method of fabricating a semiconductor device by the use of a semiconductor substrate (1), boron ions (4) are implanted into the semiconductor substrate from a trench (3) which is formed to the semiconductor substrate. The trench is defined by a plurality of side surfaces and a bottom surface extending between the side surfaces. The boron ions are implanted through all of the side surfaces and the bottom surface. It is preferable that isolating material is filled into the trench to produce a trench isolation extending over a p-well (7) and a n-well (8).

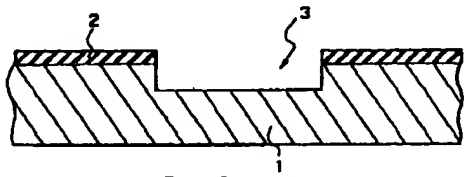

FIG. 2A

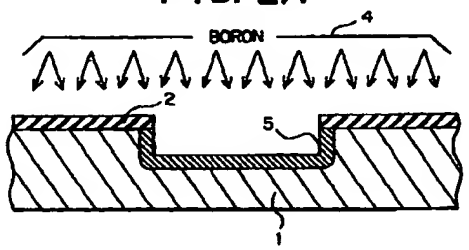

FIG. 2B

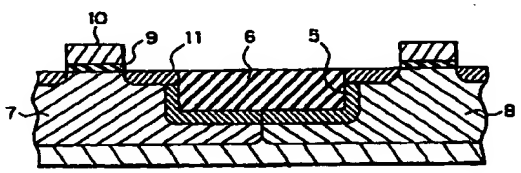

FIG. 2C

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of fabricating a semiconductor device provided with a trench isolation, particularly to a method of fabricating a semiconductor device capable of reducing an inverse narrow channel effect in which a threshold voltage lowers as the channel width of a transistor decreases in a metal oxide semiconductor field effect transistor (MOSFET).

2. Description of the Related Art

Referring to Fig. 1A description will be made about a conventional method of fabricating a semiconductor device. A trench 103 is first formed on a single-crystal silicon substrate 101, then the inner surfaces of the trench 103 are entirely oxidized through the chemical vapor deposition (CVD) method, and silicon oxide 105 is piled up as shown in Fig. 1A.

Then, as shown in Fig. 1B, the silicon oxide 105 on the surface is polished and smoothed through the chemical mechanical polishing (CMP) method and thereby, the trench 103 is filled with the silicon oxide 105, and then the surface of the silicon oxide 105 and the principal surface of the single-crystal silicon substrate 101 are covered with a gate insulating film 111 to be formed between the silicon oxide 105 and a gate electrode 110.

In this case, when the silicon oxide 105 filling the bottom of the trench 103 is lower than the principal surface of the single-crystal silicon substrate 101 as shown in Fig. 1B, a problem occurs that the threshold voltage of a MOSFET lowers by approx. 0.15 V if the channel width of the MOSFET decreases to 0.2μm from 10μm as shown by the characteristic diagram in Fig. 1C.

This is because, as described, for example, in IEDM (International Electron Devices Meeting) in 1981, Technical Digest (pp. 380-383), an electric field V in the internal direction of the single-crystal silicon substrate 101 from the gate electrode 110 and an electric field H in the direction parallel with the surface are concentrated nearby a trench shoulder 112 and then the threshold voltage of the trench shoulder 112 lowers.

That is, when the channel width of a MOSFET decreases, the rate of the portion where the threshold voltage lowers to the entire channel increases and the threshold voltage of the entire MOSFET also lowers.

To solve the above problem, there is a method of raising the threshold voltage of an edge portion of the semiconductor device by implanting impurity ions from the side surfaces of a trench.

However, because the impurity concentration becomes higher than that in the single-crystal silicon substrate 101 in the vicinity of the interface between the single-crystal silicon substrate 101 and an oxide film filling the trench 103, a junction capacity and a junction leak current are increased.

To avoid the above problem, as described in Japanese Unexamined Patent Publication No. 6-177239 (177239/1998) for example, there is a method of forming a tapered trench by etching a separation region of the semiconductor device, that is, a method of controlling the concentration of electric fields by preventing a shoulder shape from being formed at an edge portion of a semiconductor device or chamfering a shoulder.

In the case of the above conventional method of fabricating a semiconductor device, there is a problem that a phenomenon due to the reverse narrow channel effect occurs in which a threshold voltage lowers when the channel width of a transistor is too small even if using the method of controlling the concentration of electric fields by preventing a shoulder shape from being formed at an edge portion of the semiconductor device or chamfering a shoulder.

This is because the baron contained in a channel is piled up on the silicon oxide side filling a trench at the interface between the silicon of a substrate and the silicon oxide due to thermal diffusion and thereby, it diffuses outward, and a region in which the boron concentration lowers is formed nearby the interface between the trench and the substrate. The boron diffusion occurs even at approx. 800°C because inter-grid silicon is present which is produced due to ion implantation or the like.

Moreover, because phosphorus or arsenic serving as an impurity for forming an n-well is piled up on the silicon side of a substrate, it does not diffuse outward from a channel. Therefore, the above phenomenon does not occur.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a semiconductor device fabrication method in which a threshold voltage does not lower even if the channel width of a transistor decreases.

Other objects of the present invention will become clear as the description proceeds.

A method to which the present invention is applicable is of fabricating a semiconductor device including a p-well, an n-well, and a trench isolation extending over the p-well and said n-well. The method comprises the steps of preparing a semiconductor substrate and forming a trench for the trench isolation to the semiconductor substrate. The trench is defined by a plurality of side surfaces and a bottom surface extending between said side surfaces. The method further comprises implanting boron ions into the semiconductor substrate through the side surfaces and the bottom surface.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1B are sectional views showing a conventional example;

Fig. 1C is a characteristic diagram showing an example of the channel width dependency of a threshold voltage;

Figs. 2A to 2C are sectional views for explaining an embodiment of the present invention;

Fig. 3 is a characteristic diagram showing an example of the channel width dependency of the threshold voltage in Fig. 2;

Fig. 4 is a sectional view showing the second embodiment of the present invention;

Fig. 5 is a characteristic diagram showing an example of the channel width dependency of the threshold voltage in the third embodiment of the present invention;

Fig. 6 is a sectional view showing an aspect of the middle step of the present invention;

Fig. 7A is a sectional view showing the fourth embodiment of the present invention; and

Fig. 7B is a sectional view showing the fifth embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Then, an embodiment of the present invention is described below by referring to the accompanying drawings.

Figs. 2A to 2C are sectional views showing an embodiment of the present invention. In the case of the semiconductor fabrication method shown in Fig. 1A to 2C, a trench 3 is formed after the step of forming silicon oxide 2 on the principal surface of a first-conducting-type single-crystal silicon substrate 1 as shown in Fig. 2A. The trench 3 has a plurality of side surfaces and a bottom surface extending between the side surfaces.

In the next step, as shown in Fig. 2B, ions of boron 4 are implanted on the entire surfaces of the trench 3 including its wall surfaces in the diagonal direction by using the silicon oxide 2 as a mask. For example, ions of the boron 4 are implanted at a dose rate of 5E 12 cm^{-2} into the side wall of the trench 3. By the ion implantation, a boron implanted layer 5 is formed. In the case of an implantation depth, it is necessary that the peak of an impurity distribution is present at a position of approx. 50nm from the surface. For example, it is necessary that approx. 30 KeV can be applied when tilting an implantation angle by 30° from the vertical direction.

The above condition does not restrict the present invention. Conditions can be changed in accordance with a case in which a different implantation angle is used or a mask of silicon oxide is formed on the surfaces of a trench.

Then, as shown in Fig. 2C, the trench 3 is filled with isolating material of silicon oxide 6 to produce the trench isolation described before. The principal surface of the substrate 1 in a range excepting the silicon oxide 6 is exposed by the step of surface polishing, and impurity ions for respectively forming a p-well 7 and an n-well 8 are implanted to form source-drain 11 through annealing. Baron is accelerated and diffused by the inter-grid silicon produced in the above steps, mainly in the ion implantation step and the concentration lowers. However, because only the boron corresponding to the quantity first implanted into the entire surface outward diffuses into a silicon oxide 6 filling the trench 3, the boron concentration of the p-well 7 does not lower to a predetermined concentration or less nearby the interface between the single-crystal silicon substrate 1 and the trench 3. Therefore, the reverse narrow channel effect does not occur.

Fig. 2C further shows a state of completing the step of forming a gate insulating film 9 and a gate electrode 10.

Moreover, Fig. 3 is a characteristic diagram showing the channel-width dependency of a MOSFET threshold voltage in accordance with the step described by referring to Figs. 2A to 2C. As shown in Fig. 3, threshold voltages hardly change even if channel widths change.

Then, the second embodiment different from the embodiment shown in Figs. 2A to 2C is described below by referring to Fig. 4.

In Fig. 2C, it is preferable to outward diffuse the boron in the region for the n-well 8 in the direction of the silicon oxide 6 in the trench. Therefore, as shown in Fig. 4, when implanting ions into the n-well 8, it is necessary to increase the amount of inter-grid silicon by using photoresist 12 as a mask and thereby additionally implanting silicon 13. In this case, a dose rate of 1E 14 cm^{-2} or more is preferable.

Then, the third embodiment having the characteristic in Fig. 5 is described below.

Fig. 5 is a characteristic diagram in which phosphorus ions are additionally implanted when implanting boron ions into the entire surface shown in Fig. 2B. Phosphorus ions are implanted at the energy realizing a depth almost equal to the case of boron ions and at a dose rate equal to or up to two times larger than that of boron. In the case of this method, the reverse narrow channel effect remains. However, even if the channel width decreases from 10μm to 0.2μm, the threshold voltage decreases only by approx. 0.08 V and a great improvement of the characteristic is confirmed compared to the conventional characteristic shown in Fig. 1C.

This advantage is also obtained by using arsenic instead of phosphorus. Moreover, the same advantage can be also obtained by combining phosphorus with arsenic. Even if these elements are implanted before or after the boron implantation step, the improved advantage is the same.

Moreover, as shown in Fig. 6, it is also effective to

selectively implant boron ions only into the p-well 7. In this case, as shown in Fig. 6, it is necessary to cover only the n-well 8 with photoresist 14 and implant boron ions after the step of forming the trench 3. However, if the separation width is too small in this step, boron cannot be diagonally implanted because it is shaded by the photoresist 14.

Figs. 7A and 7B are views of the fourth and fifth embodiments showing the shapes of photoresists 15 and 16 used to avoid the problem caused in Fig. 6.

In Fig. 7A, the photoresist 15 whose shoulder is rounded is formed by forming the photoresist 14 in Fig. 6 and thereafter annealing it at a temperature at which it flows. As a result, the shaded area for ion implantation is decreased.

Moreover, in Fig. 7B, an advantage same as the above mentioned is obtained by forming the photoresist 14 in Fig. 6 and then, anisotropically etching it to form a side wall made of the photoresist 16 on the wall surface of the trench.

One of the problems is that the semiconductor substrate has an edge portion. To avoid such the problem, the method comprises a step of chamfering the edge portion before the above-described steps.

The above-described step is incorporated into other steps. As long as the above function is satisfied, it is free to replace preceding and following steps each other or perform simultaneous processing. Therefore, the above description does not restrict the present invention.

As described above, the present invention makes it possible to obtain an advantage that the reverse narrow channel effect of a semiconductor device using a trench isolation can be decreased.

This is because boron ions are implanted into the entire surface of a trench after the trench is formed and thereby, the amount of boron equivalent to a value of lowered concentration can be compensated by thermally outward diffusing the boron toward the silicon oxide for filling the trench.

The present invention is particularly effective for the reverse channel effect of an n-MOSFET. According to the embodiments, it is possible to reduce the standby current of a semiconductor integrated circuit by 30%.

Claims

1. A method of fabricating a semiconductor device including a p-well (7), an n-well (8), and a trench isolation extending over said p-well and said n-well, said method comprising the steps of preparing a semiconductor substrate (1) and forming a trench (3) for said trench isolation to said semiconductor substrate, said trench being defined by a plurality of side surfaces and a bottom surface extending between said side surfaces, characterized in that said method further comprising the step of implanting boron (4) ions into said semiconductor substrate through said side surfaces and said bottom surface.

2. A method as claimed in claim 1, further comprising the step of implanting silicon into a region for said n-well in the first-mentioned implanting step.

3. A method as claimed in claim 1, wherein the implanting step comprises the steps of:

   implanting one kind of said boron ions and phosphorus ions into said semiconductor substrate; and then
   implanting another kind of said boron ions and phosphorus ions into said semiconductor substrate.

4. A method as claimed in claim 1, wherein the implanting step comprises the steps of:

   implanting one kind of said boron ions and arsenic ions into said semiconductor substrate; and then
   implanting another kind of said boron ions and arsenic ions into said semiconductor substrate.

5. A method as claimed in claim 1, wherein the implanting step comprises the steps of:

   implanting any one kind of said boron ions, phosphorus ions, and arsenic ions into said semiconductor substrate; then
   implanting one of two other kinds of said boron ions, phosphorus ions, and arsenic ions into said semiconductor substrate; and then
   implanting the other kind of said boron ions, phosphorus ions, and arsenic ions.

6. A method as claimed in claim 1, further comprising the step of covering a region for said n-well with photoresist (14) before the implanting step.

7. A method as claimed in claim 6, further comprising the step of reflowing said photoresist to produce reflowed photoresist before the implanting step.

8. A method as claimed in claim 7, further comprising the step of selectively etching a part of said reflowed photoresist to leave another part of said reflowed photoresist on said side surfaces of the trench.

9. A method as claimed in claim 1, wherein said semiconductor substrate has an edge portion, said method further comprising the step of chamfering said edge portion before the forming step.

10. A method as claimed in claim 1, wherein said semiconductor substrate has a principal surface on

which said trench is opened, said semiconductor substrate including a trench shoulder portion which is defined by said principal surface and each of said side surfaces of the trench, said method further comprising the step of rounding said trench shoulder portion before the implanting step.

11. A method as claimed in claim 1, wherein said semiconductor substrate has a principal surface on which said trench is opened, said method further comprising the step of filling isolating material in said trench to protrude over said principal surface after the implanting step, the filling step resulting in producing said trench isolation.

12. A method as claimed in claim 1, wherein said semiconductor substrate is made of a first-conducting-type single-crystal silicon substrate.

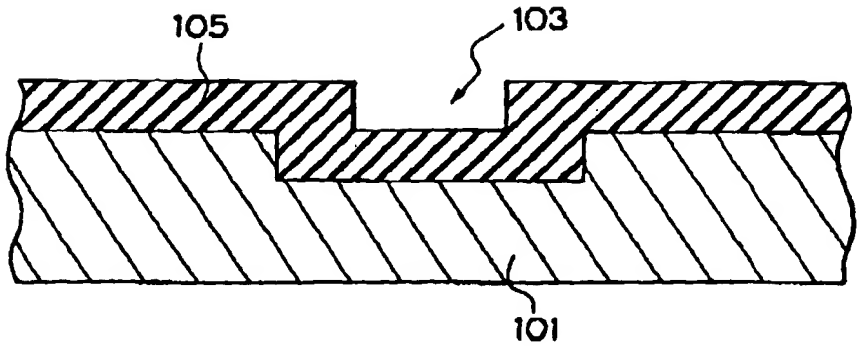

FIG. 1A PRIOR ART

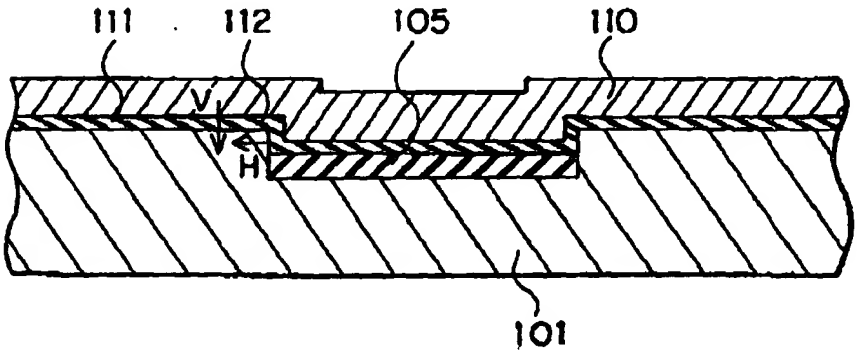

FIG. 1B PRIOR ART

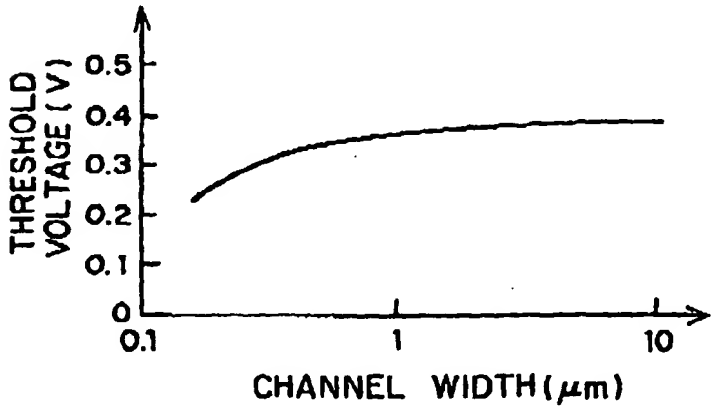

FIG. 1C PRIOR ART

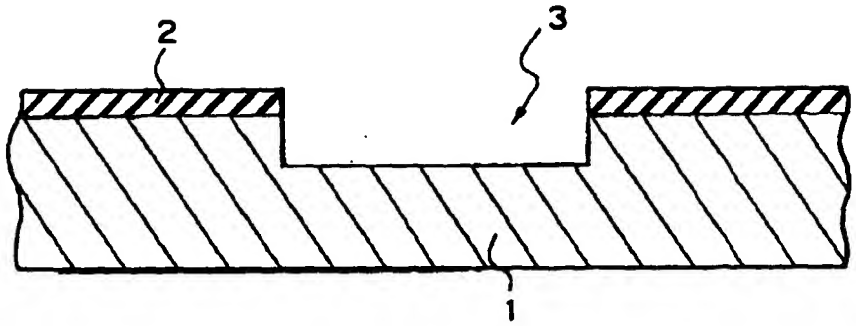

FIG. 2A

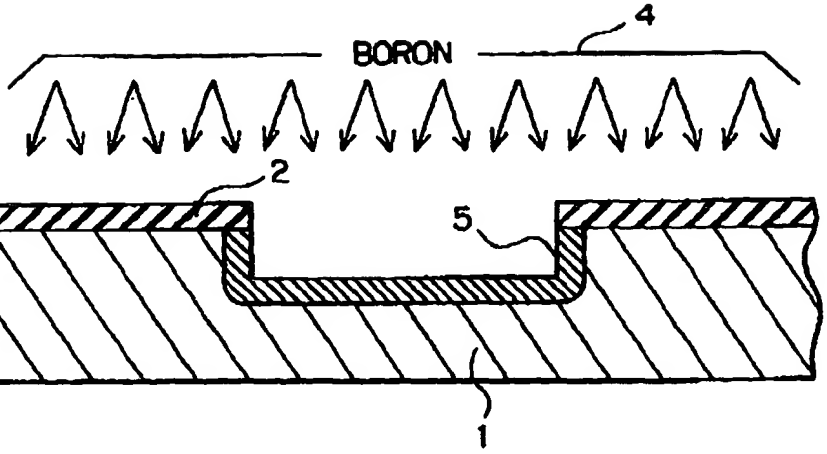

FIG. 2B

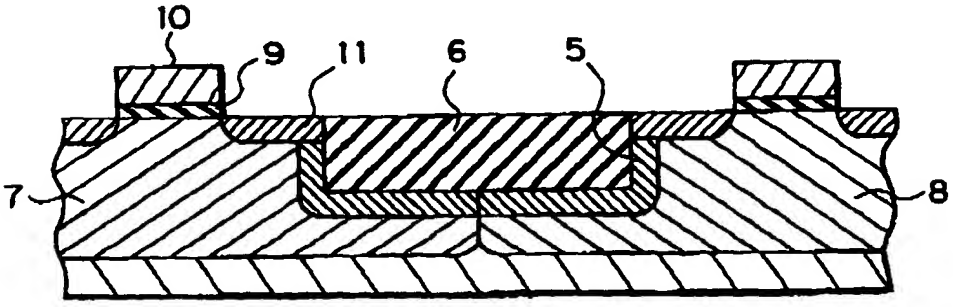

FIG. 2C

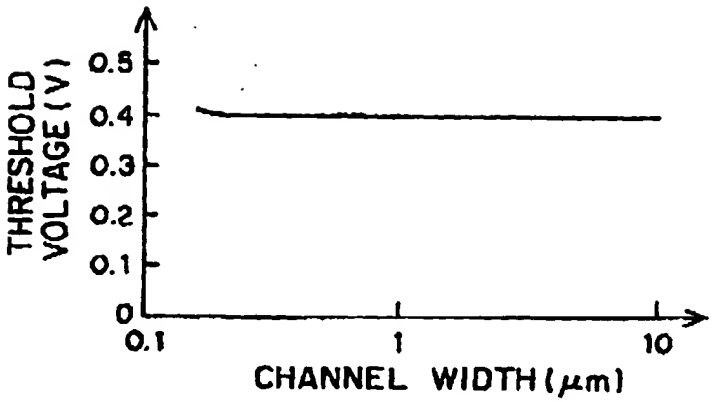
THRESHOLD VOLTAGE (V)
0.5
0.4
0.3
0.2
0.1
0
0.1
1
10
CHANNEL WIDTH (μm)

FIG. 3

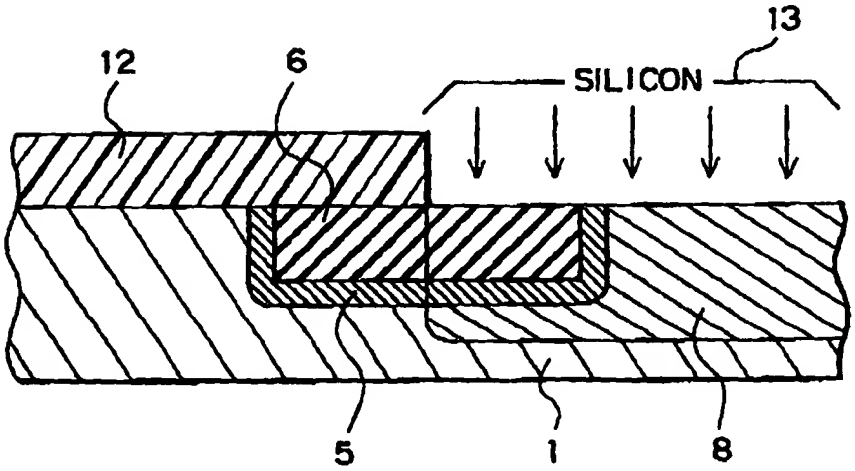
13
12
6
SILICON
5
1
8

FIG. 4

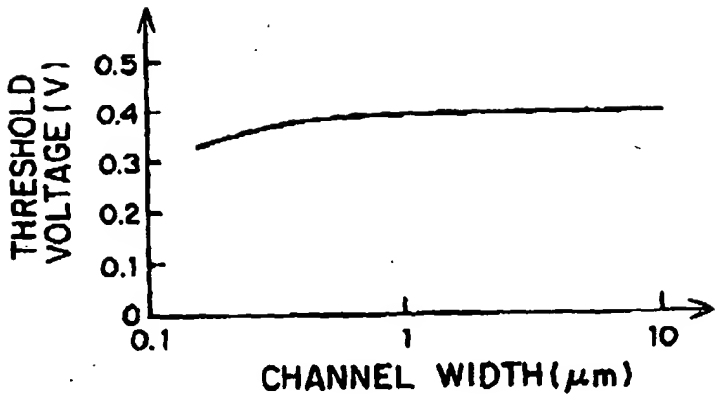
THRESHOLD VOLTAGE (V)
0.5
0.4
0.3
0.2
0.1
0
0.1
1
10
CHANNEL WIDTH (μm)

FIG. 5

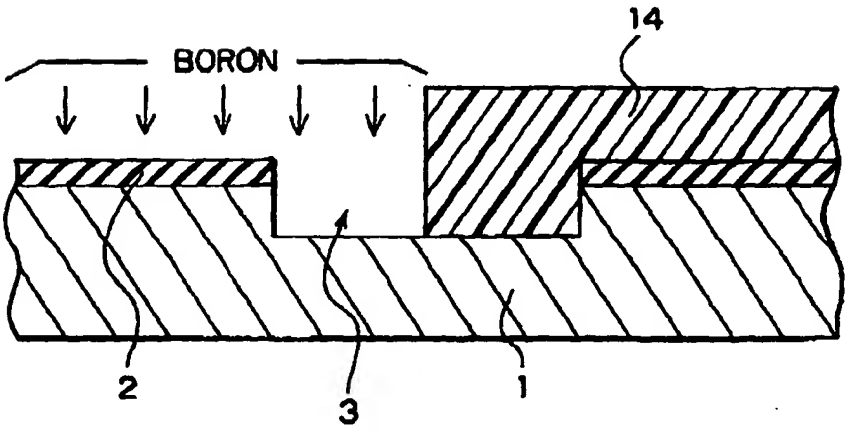
BORON
14
2
3
1

FIG. 6

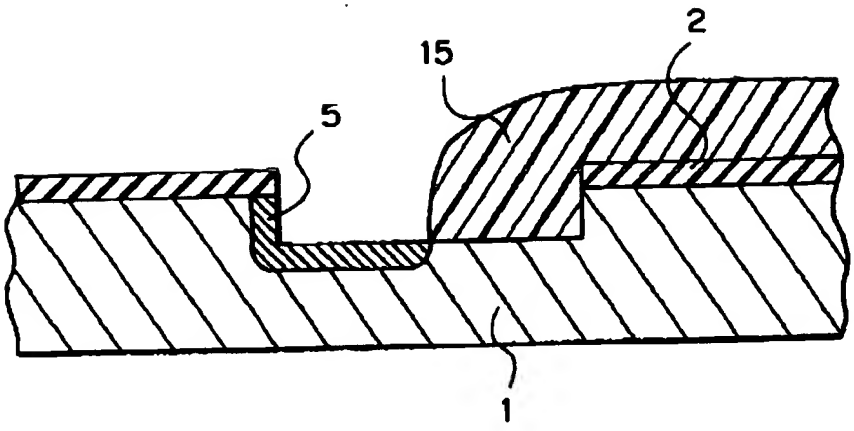

FIG. 7A

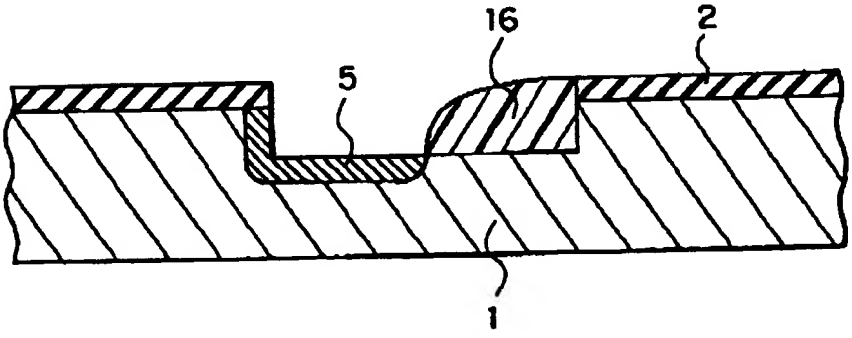

FIG. 7B

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 10 9227

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	WO 87 00687 A (AMERICAN TELEPHONE & TELEGRAPH) 29 January 1987 * abstract; figure 6 * * page 7, line 19 - line 22 *	1,12	H01L21/762 H01L21/265
A	US 4 918 027 A (FUSE GENSHU ET AL) 17 April 1990 * abstract; claims; figures *	1,12	
A	EP 0 399 066 A (SEIKO EPSON CORP) 28 November 1990 * abstract; claims; figure 6 *	1,9,10, 12	
A	EP 0 731 494 A (ADVANCED MICRO DEVICES INC) 11 September 1996 * abstract; claims; figures * * column 6, line 35 - column 8, line 11 *	1-5	
A	US 4 534 824 A (CHEN PAU-LING) 13 August 1985 * abstract; figures 25,26 *	1,6-8,11	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
A	PATENT ABSTRACTS OF JAPAN vol. 008, no. 119 (E-248), 5 June 1984 & JP 59 032125 A (HITACHI SEISAKUSHO KK), 21 February 1984 * abstract *	1,6-8	H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 August 1998	Wirner, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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